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(54) Operational amplifier arrangement including a quiescent current control circuit

(57) A method for controlling the quiescent output current of an operational amplifier arrangement (OAA) by means of tuning offset voltages of a stage (A2,A3) preceding a differential output driver stage (OS), further includes a step of selecting the cut-off frequency of the filter formed by the input capacitors of said differential output driver stage (OS) and the output impedance of said stage (A2,A3) preceding said differential output driver stage (OS), such that said cut-off frequency is lower than a predetermined part of the maximum bandwidth of the input signal (vin) applied to said operational amplifier arrangement (OAA), and whereby said stage (A2,A3) preceding said differential output driver stage (OS) is designed such as to be limited in output swing. The invention relates as well to an operational amplifier designed in accordance with the subject methodology.

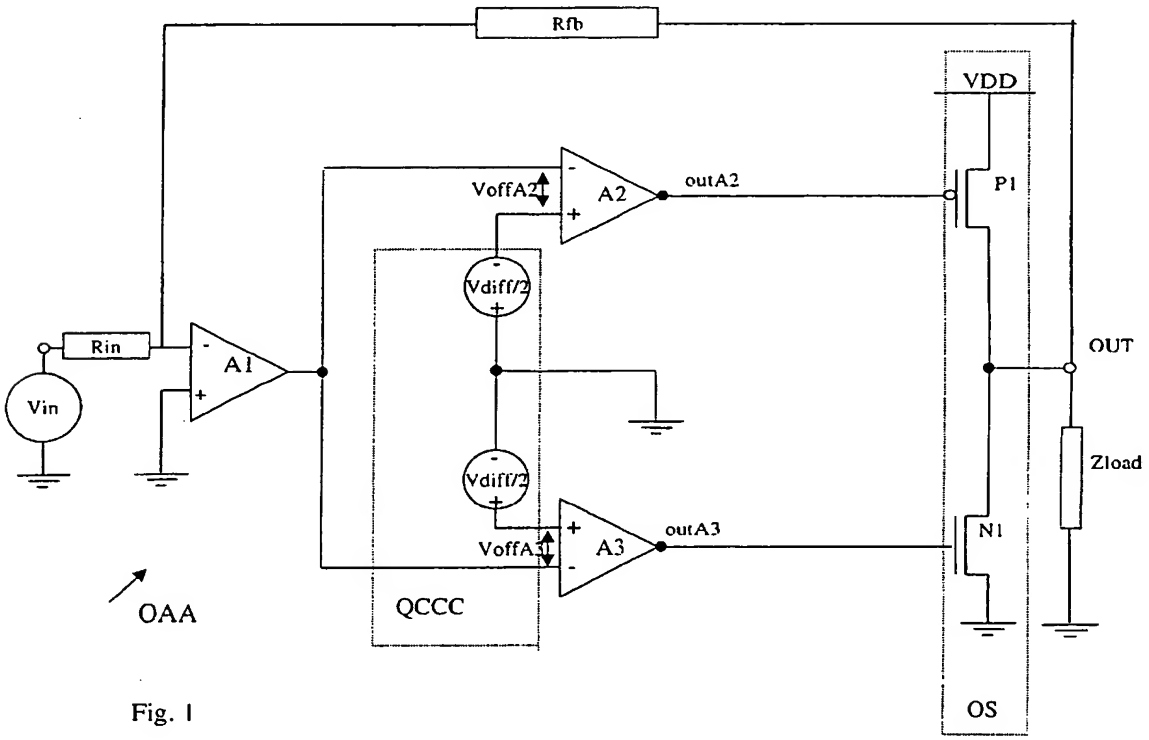

Fig. 1

EP 1 258 981 A1

Description

[0001] The present invention relates to a method for controlling the quiescent current of an operational amplifier arrangement as is described in the non-characterising portion of the first claim, and to an operational amplifier arrangement which is adapted to perform such a method as is described in the non-characterising portion of claim 2 .

[0002] Such a method and amplifier arrangement to control the quiescent current are already known in the art, e.g. from the article *"A 3.3 V Low-distortion* ISDN *Line Driver with a Novel Quiescent Current Control Circuit", written by H. Casier, P. Wouters, B. Graindourze and D. Sallaerts, IEEE Journal of Solid-State Circuits, Vol. 33, Nr 7, July 1998*, pp. 1130- 1133. Therein, on page 1132, an amplifier arrangement including a quiescent current control circuit is shown and described. Basically the currents flowing in each of the two output branches of the output stage of the operational amplifier are sensed and compared in a comparator, which consists of a simple inverter and a phase detector. Comparison with a reference current Iref is performed. The output of the comparator is fed back to the input stage of the amplifier arrangement via a charge pump circuit which charges or discharges a hold capacitor, dependent on this comparator output signal : if both sensed output currents are higher than the target reference or quiescent current, the capacitor is discharged ; if both sensed output currents are lower than the target quiescent current, the capacitor is charged. The charge on the capacitor is further transformed via a buffer and attenuator, into a voltage difference between the positive input terminals of both error amplifiers preceding the output stage. This voltage difference, corresponding to the quiescent offset voltage, can be considered as a change in the input offset voltage of both amplifiers.

[0003] A drawback of this prior art method is however that the quiescent current level is set statically, thus without any frequency dependency. Therefore the quiescent current has to be dimensioned for the worst-case signal, i.e. the input signal which is the highest in frequency. This however results in a waste of power, as the quiescent current is thereby over-dimensioned for the lower frequency signals.

[0004] An object of the present invention is to provide a method for controlling the quiescent current of an operational amplifier arrangement, but whereby the quiescent current is set such as to be dependent on the frequency of the input signal .

[0005] According to the invention, this object is achieved due to the fact that the method further includes the steps as described in the characterizing portion of the first claim and that said operational amplifier arrangement is further adapted as is described in claim 2.

[0006] In this way, the cut-off frequency of the inherent filter which is formed by the input capacitors of the transistors of the differential output stage and the output impedance of the previous stage, is selected or designed such that this is lower than the maximum frequency of the input signal. In combination with the fact that this previous stage is limited in output swing, a higher quiescent output current for the frequencies that lie beyond this cut-off frequency is achieved. Input signals having higher frequencies will thus result in a higher quiescent current. The static power budget can thus be reduced by more than 50% compared to an equivalent non-dynamic control architecture.

[0007] Another characteristic feature of the present invention is described in claim 3.

[0008] Thereby the stage preceding the differential output stage can be chosen as to have a very simple architecture. Similarly, the differential output stage is a class AB amplifier as stated by claim 4, which can also have a very simple architecture.

[0009] It is to be noticed that the term 'coupled', used in the claims, should not be interpreted as being limitative to direct connections only. Thus, the scope of the expression 'a device A coupled to a device B' should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means.

[0010] It is to be noticed that the term 'comprising', used in the claims, should not be interpreted as being limitative to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0011] The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

FIG. 1 represents a schematic of a general amplifier arrangement wherein the method of the invention is realized ,

Fig. 2 represents a transistor schematic implementation of the amplifiers A2 and A3 together constituting the stage preceding the output stage and which are shown in Fig. 1,

Fig. 3 shows simulation results of the output voltages of the preceding stage for low and high frequencies for a particular example, and

Fig. 4 shows simulation results of the quiescent current obtained at low and high frequencies for this particular example .

[0012] The operational amplifier arrangement as depicted in Fig. 1 is for instance used in ADSL or VDSL or, in general xDSL line drivers . ADSL is the abbreviation of asymmetric digital subscriber line whereas VDSL is

the abbreviation of very high speed digital subscriber line . xDSL thereby stands for all possible digital subscriber line applications.

[0013] The requirements in these xDSL applications are very stringent : high bit rate, long reach, less than 10E-7 bit error rate, which translates itself into severe requirements for noise and distortion performance. Furthermore the input signals show a high Crest factor, being the ratio between the peak and the RMS voltage on the line.

[0014] Therefore the control of the quiescent current level of the output stage has to be done very accurately, and preferably being insensitive to process and temperature variations.

[0015] On the other hand power consumption needs to be minimized as much as possible, whereas influence on the signal path has to be avoided.

[0016] Furthermore it is desirable that this quiescent current should be dynamically controllable . Indeed, dynamically controlling the quiescent current allows for a higher quiescent current level where needed by increasing the quiescent current level as a function of the input and thus also of the amplified signal frequency. By increasing the quiescent current at higher frequencies, the distortion level at these higher frequencies is reduced in an efficient way. In addition the overall power consumption is substantially reduced, since the quiescent current level will only be selectively increased for the signals in the higher frequency range. This is in contrast to the known static quiescent current control techniques which all aim at a preset target level for the quiescent current for all frequencies. With a dynamic quiescent current control technique it is possible to set a lower quiescent current for the lower frequency signals and a higher quiescent current for the higher frequency signals, thereby reducing overall power consumption. The higher quiescent currents are desirable at these higher frequencies for distortion reasons : due to the dominant pole of the operational amplifier, the loop gain will decrease at the higher frequencies. The result is that the distortion at these higher frequencies will also be higher . This can however be overcome by a higher quiescent current at these higher frequencies.

[0017] The operational amplifier arrangement and the quiescent current control method of the present invention are thereby capable of providing a solution to the aforementioned requirements as will be explained below.

[0018] The operational amplifier arrangement depicted in Fig. 1 includes a common input stage A1 which is receiving the input signal, for instance the D/A converted ADSL signal as received from a processor. The output terminal OUT of this operational amplifier arrangement is then coupled to the load which can consist of the line impedance in case of the aforementioned ADSL signal. The load impedance that is driven by the output amplifier and is coupled to the output terminal of the amplifier arrangement, is denoted with Zload in Fig. 1.

[0019] For linearity and stability reasons this output signal is fed back to the input of the common input stage A1 via a feedback circuit, indicated as Rfb .

[0020] The output terminal of A1 is coupled to input terminals of two offset amplifiers A1 and A2, which together form the stage preceding the final differential output driver stage OS. Because of the stringent linearity reasons for xDSL output amplifiers, OS consists of a class AB amplifier for these applications. However the invention is as well applicable to other types of output amplifiers. A class AB amplifier, in its simplest form, basically consists of a p-type transistor P1 in series with an n-type transistor N1. In the embodiment depicted in Fig. 1 both P1 and N1 are CMOS transistors, but implementations in other technologies such as bipolar technologies are also possible.

[0021] The quiescent current is defined as the current which is flowing in the output stage OS when no input signal Vin is applied. Such a current originates from the DC bias conditions. Since variations on this current directly add to the power consumption in the load ZLOAD, the value of the quiescent current has to be set as accurate as possible. This is the function of a Quiescent Current Control Circuit, abbreviated with QCCC, and which, in its most basic form, includes circuitry for adjusting the input offset voltages VoffA2 and VoffA3 of the two differential amplifiers A2 and A3 of the stage preceding the differential output driver stage. This circuitry is schematically depicted as two voltage sources, Vdiff2 and Vdiff3 in Fig. 1, and may consist in one embodiment of the present invention of D/A convertors. The quiescent current control circuit may in more complex embodiments further include other circuitry for adaptively tuning these offset levels, based on a measurement of the output currents. These circuits are for instance described in the already mentioned prior art article.

[0022] These presently known quiescent current control circuits however do not dynamically control the quiescent current. A dynamic regulation is achieved by a following a particular design methodology for both the differential output driver stage OS and the stage preceding this output driver stage. This design is thereby such that the cut-off frequency of the filter which is formed by the input capacitors of the input transistors of the output stage, and the output impedance of the stage preceding this output stage, is lower than a predetermined percentage of the maximum bandwidth of the input signal. Dependent on the specific requirements, this predetermined percentage can be chosen as 70, 80 or even 100 %, as being influenced by external requirements such as the distortion specification. In an example of an ADSL line driver that has a signal bandwidth of approximately 140 KHz and a distortion specification of smaller than -- 70 dB for a 100 kHz sine wave input, this cut-off frequency is set at to be at 50 KHz.

[0023] The target for the constant quiescent current setting at low frequencies is set at 5mA for this application.

[0024] An additional and mandatory design feature for the dynamic behaviour of the quiescent current control is that the stage preceding the output stage, has to be limited in output swing. Herewith is meant that the output signal provided by these amplifiers is clipping to the supply voltages, for the higher input voltages received by these amplifiers. The level of clipping can be chosen and is not limitative to the design methodology. A simple transistor embodiment realising such a stage of which the amplifiers are limited in output swing, is shown in Fig. 2. Therein an embodiment for the differential amplifiers A2 and A3 are shown. It is to be remarked that, although CMOS transistor embodiments are shown, an embodiment whereby the nMOS transistors are replaced by npn bipolars, and whereby the pMOS transistors are replaced by pnp bipolars, is as well possible.

[0025] Differential amplifier A2 thereby basically consists of a differential transistor pair of transistors T3 and T4, in a common-emitter or common-source circuit scheme. For T3 and T4 being nMOS transistors, their sources are coupled together to one terminal of a current source Is. Another terminal of that current source is coupled to the ground reference terminal.

[0026] The drains of transistors T3 and T4 are coupled via a resistive load to the supply voltage terminal VDD. In the embodiment depicted in Fig. 2, these resistive loads are realised by means of respective transistors T1 and T2. The drain terminal of T4 further serves as the output terminal of amplifier A2.

[0027] A similar transistor level embodiment is shown in Fig. 2 for amplifier A3 .

[0028] Because of the limited output swing of amplifiers A2 and A3 they cannot compensate for the loss that is caused by the inherent filter. Basically the overall amplifier wants to make sure it is presenting the correct voltages to the gates of N1 and P1 of the output driver stage, such as to ensure the proper quiescent current levels. To reach this goal the amplifiers A2 and A3 have to compensate for the loss caused by the filer, by further boosting up their output swing. In the direction of the output signal towards the analog ground, which is lying in between the supply voltage and the ground potential, the output transistors are completely turned on, and there is no problem. In the direction of the output swing towards the supply and the ground potential however, the transistors TN2 and TP2 output levels of A3, resp, A2, clip to the minimum ground and maximum supply voltage level respectively. Therefore the output of amplifiers A2 and A3 is no longer following the ideal behaviour, and can not longer follow turning on and off N1 and P1 of the differential output stage as is required to keep the quiescent current constant at the target value. The result of this is that the quiescent current increases, whereby this effect is more pronounced at higher frequencies.

[0029] This can be seen at the plots of Fig. 3 where the output voltages of A2 and A3 are shown for input signals with a low frequency, denoted by low f, of 10 KHz and a high frequency, denoted by high f, and being 100 kHz resp. The top figure of Fig. 3 showns simulation results of an ideal operational amplifier, for which no clipping should occur, and the results for the amplifiers A2 and A3 of Fig. 2, for 10 KHz. The result for the ideal A2 amplifier is denoted by " Pdrive-output_ideal", for the ideal A3 amplifier by "Ndrive_output_ideal", and the actual A2 by "Pdrive_output_actual" and the actual A3 by "Ndrive_output_ideal". The bottom plot of Fig. 3 uses the same nomenclature, but shows the results for the 100 KHz, thus the high frequency case. For the 10 KHz case the output voltage is still forming a sinewave trajectory, whereas for the 100 KHz case the clipping is clearly observed . Fig. 4 shows the quiescent current levels for the same input signals, both for the 10KHz and the 100KHz cases. Again the quiescent currents are also shown, and denoted by means of "Iqn_ideal" and "Iqp_ideal" respectively. From this figure it is clear that for the 10 KHz input signal the target quiescent current of 5 mA is reached. This target corresponds to the quiescent current for an ideal amplifier A2 and A3, thus these without the clipping behaviour. However for the 100 KHz input signal this level goes up to 33 and 22 mA, depending on the falling or rising edge in the sine waveform .

[0030] The design methodology which is thus generally followed is to first determine the needed minimum quiescent current level for the highest signal frequencies in order to obtain the same distortion levels as for the lower signal frequencies, given a target quiescent current for these lower frequencies. Next the cut-off frequency is chosen such as to guarantee the above mentioned quiescent current level for the higher frequency band and the filter characteristics are iteratively determined, usually by means of simulations, such as to obtain this desired value of the maximum quiescent current level. In general, and also in the specific ADSL output amplifier example described above, the dimensions of the output transistors are mainly determined via their current and voltage swing. From these dimensions, the input capacitance automatically follows. Given the cut-off frequency of the filter, the output impedance of the previous stage can then be automatically calculated after which step this previous stage can then be further tuned such as to obtain this output impedance value.

[0031] While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention, as defined in the appended claims.

Claims

1. Method for controlling the quiescent output current of an operational amplifier arrangement (OAA), said method including the steps of tuning respective input offset voltages of a stage (A2,A3) preceding a

differential output driver stage (OS),

characterized in that

said method includes a step of selecting the cut-off frequency of the filter formed by the input capacitors of said differential output driver stage (OS) and the output impedance of said stage (A2,A3) preceding said differential output driver stage (OS), such that said cut-off frequency is lower than a predetermined part of the maximum bandwidth of the input signal (vin) applied to said operational amplifier arrangement (OAA),

and whereby said stage (A2,A3) preceding said differential output driver stage (OS) is designed such as to be limited in output swing.

2. Operational amplifier arrangement (OAA) including a differential output stage (OS), input terminals of which are coupled to respective output terminals of a stage (A2,A3) preceding said differential output stage (A2,A3), said operational amplifier arrangement (OAA) further including a quiescent current control circuit (QCCC) adapted to control the quiescent current of said differential output driver stage (OS) by tuning respective input offset voltages (VoffA2, VoffA3) of said stage preceding said differential output stage (OS)

characterized in that

the filter formed by the output impedance of said stage (A2,A3) preceding said differential output driver stage (OS), and the input capacitors of said differential output stage (OS), has a cut-off frequency which is lower than a predetermined part of the maximum bandwidth of the input signal (vin) of said operational amplifier arrangement (OAA),

and said stage (A2,A3) preceding said differential output driver stage (OS) is limited in output swing.

3. Operational amplifier arrangement (OAA) according to claim 2

characterized in that

said stage (A2,A3) preceding said differential output driver stage includes a pair of differential amplifiers, a differential amplifier of said pair thereby including a differential pair of transistors, in a common emitter circuit coupled to a current source, the collector output terminals of both transistors of said differential pair being coupled via a load to the supply voltage .

4. Operational amplifier arrangement (OAA) according to claim 2

characterized in that

said differential output driver stage (OS) consists of a class AB output driver.

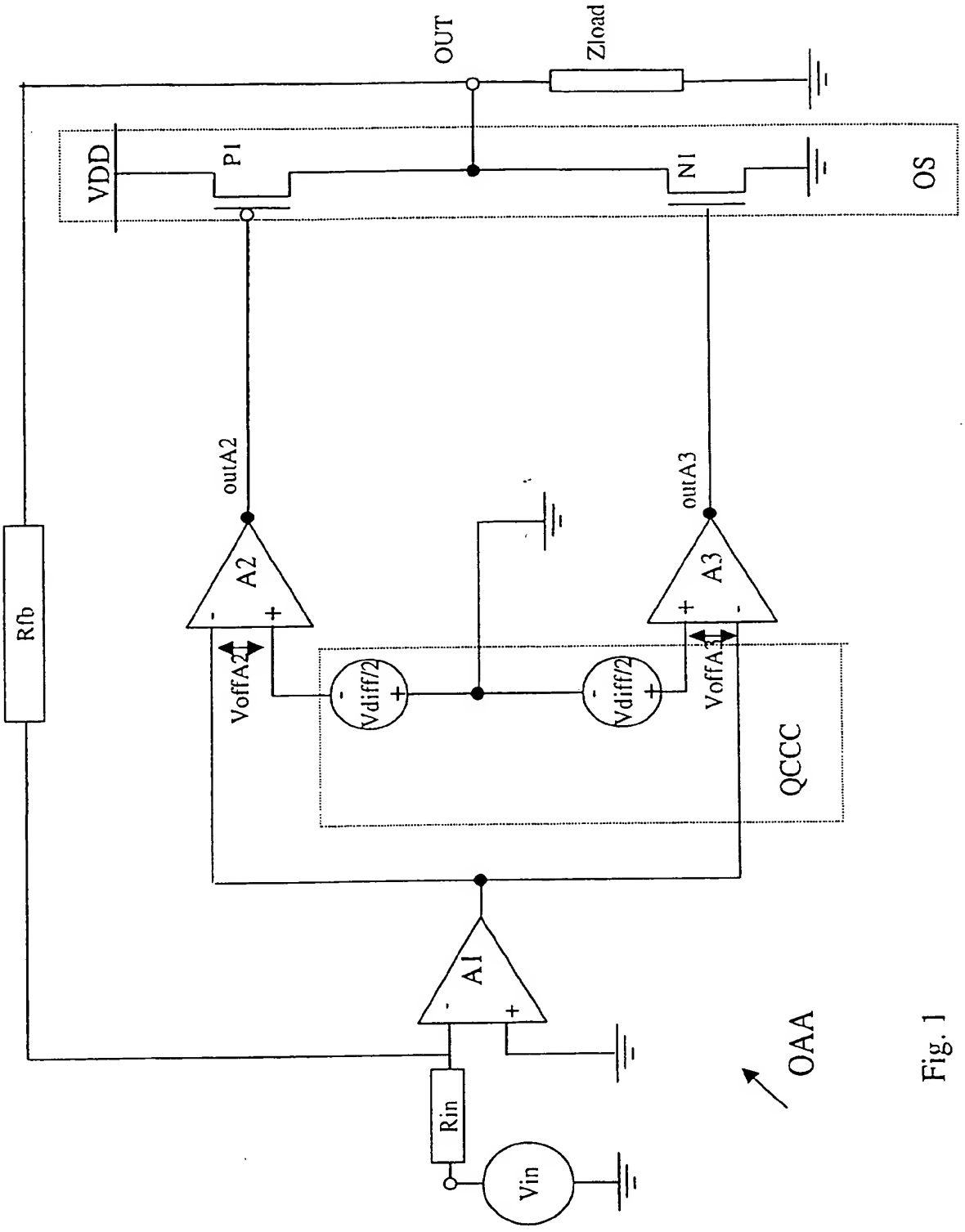

Fig. 1

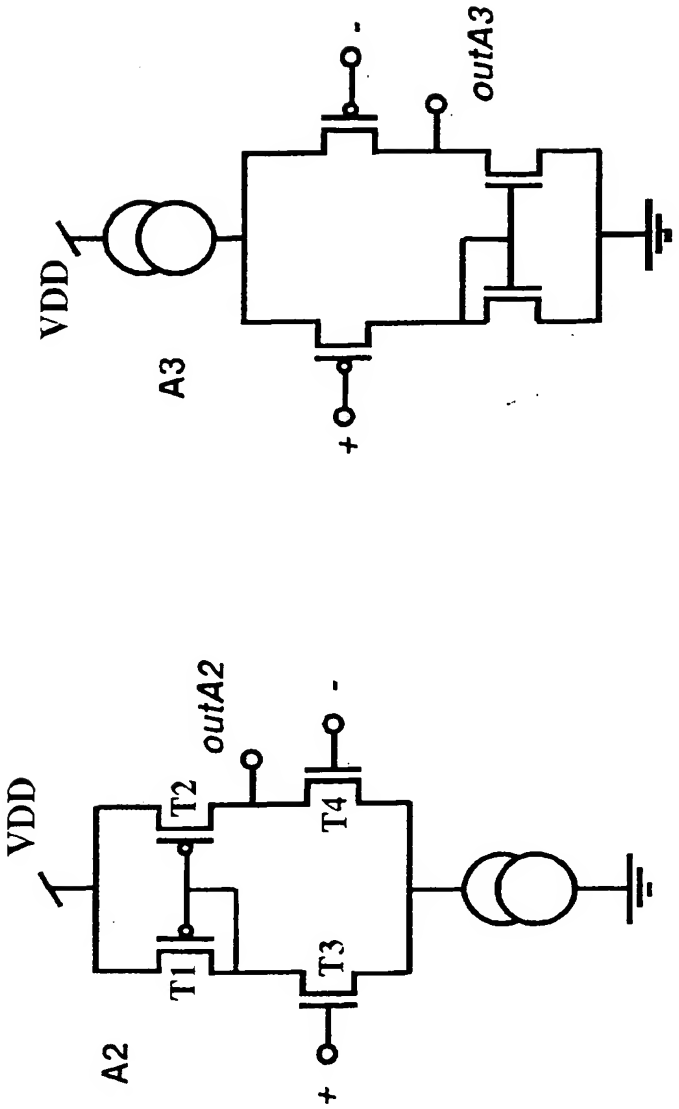

Fig. 2

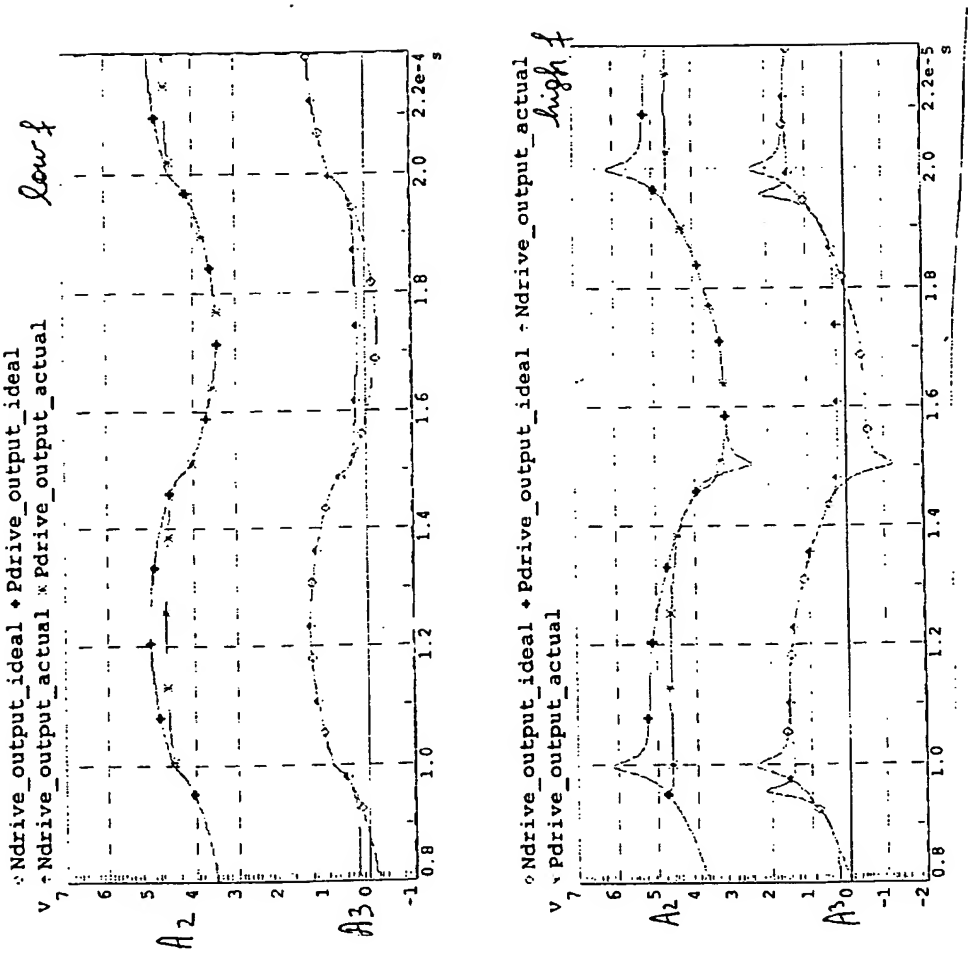

Fig. 3

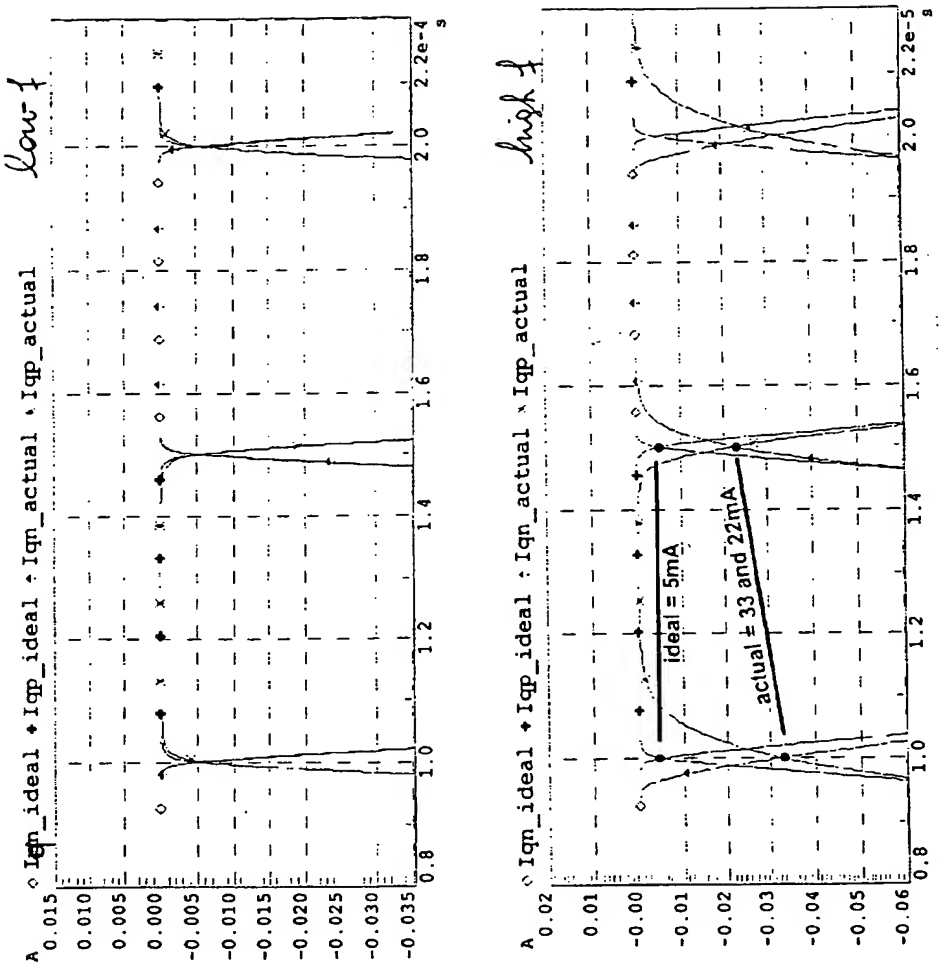

Fig. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 01 40 1312

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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 November 2001	Segaert, P

CATEGORY OF CITED DOCUMENTS

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